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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,757	12/17/2001	Hyung-Jun Kim	P67358US0	7540

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,757	KIM, HYUNG-JUN	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed January 22, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5, 6, 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as obvious over Kim et al. (U.S. Patent No. 5,534,728).

In regards to claim 1, Kim et al. ("Kim") discloses the following:

a) a plurality of metal wire patterns which include a fine line pattern and pad patterns (For Example: See Figure 4).

In regards to claim 1, Kim fails to disclose the following:

a) an area of the fine line pattern being more than 1% of a total area of said plurality of metal wire patterns.

Although Kim does not explicitly state that the fine line pattern is more than 1% of a total area of said plurality of metal wire patterns, the Examiner is permitted to give a claim the broadest reasonable interpretation consistent with the specification. See MPEP § 2111. The claim fails to describe a definitive area of the fine line pattern in relation to the overall layout of

the metal wire patterns. Additionally, it is true that Kim does not explicitly state that the area of the fine line pattern is more than 1% of a total area of plurality of metal wire patterns, however it is clear that Kim shows a fine line pattern-metal wire pattern orientation in the same manner as claimed. It would have been obvious to one of ordinary skill in the art to allocate the claimed pattern ratio to establish electrical communication between the chip and peripheral components since such technology was well known in the art at the time the invention was made.

In regards to claim 3, Kim discloses the following:

a) the pad patterns include connection pad patterns which electrically connect the pad patterns to the fine line pattern, said connection pad patterns being included in said total area (For Example: See Figure 4).

In regards to claim 5, Kim discloses the following:

a) a plurality of metal wire patterns which include main fine line patterns, main pad patterns and dummy fine line patterns (For Example: See Figure 4).

In regards to claim 5, Kim fails to disclose the following:

a) an area of the dummy fine line patterns, which are connected to the pad patterns, being less than 1% of a total area of said plurality of metal wire patterns and also being less than a value obtained by dividing an area of the main fine line patterns by said total area.

Although Kim does not explicitly state that an area of the dummy fine line patterns, which are connected to the pad patterns are less than 1% of a total area of said plurality of metal wire patterns and less than a value obtained by dividing an area of the main fine line patterns by said total area, the Examiner is permitted to give a claim the broadest reasonable interpretation consistent with the specification. See MPEP § 2111. The claim fails to describe a definitive area of the dummy fine line pattern in relation to the overall layout of the metal wire patterns. Additionally, it is true that Kim does not explicitly state that an area of the dummy fine line patterns, which are connected to the pad patterns are less than 1% of a total area of said plurality

of metal wire patterns and less than a value obtained by dividing an area of the main fine line patterns by said total area, however it is clear that Kim shows a dummy fine line pattern-metal wire pattern orientation in the same manner as claimed. It would have been obvious to one of ordinary skill in the art to allocate the claimed pattern ratio to establish electrical communication between the chip and peripheral components since such technology was well known in the art at the time the invention was made.

In regards to claim 6, Kim discloses the following:

a) the dummy fine line patterns are formed parallel with the main fine line patterns at a distance of a width of the main fine line pattern (For Example: See Figure 4).

In regards to claim 8, Kim discloses the following:

a) the dummy fine line patterns do not form or contribute to any electric circuit (For Example: See Abstract).

In regards to claim 9, Kim discloses the following:

a) the plurality of metal wire patterns further include dummy pad patterns, to which the dummy fine line patterns are connected, said dummy pad patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns (For Example: See Abstract and Figure 4).

In regards to claim 10, Kim discloses the following:

a) the plurality of metal wire patterns further include dummy pad pool patterns, to which the dummy fine line patterns are connected, said dummy pad pool patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns (For Example: See Abstract and Figure 4).

In regards to claim 12, Kim discloses the following:

a) the plurality of metal wire patterns further include connection pad patterns which electrically connect the main pad patterns to the fine line patterns, said connection pad patterns being included in said total area (For Example: See Abstract and Figure 4).

In regards to claim 13, Kim fails to disclose the following:

a) the total area is represented by Ap+Ac+A+d, where, 'd' represents the area of the dummy fine line patterns, 'Ap' represents an area of the main pad patterns, 'Ac' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns.

Although Kim does not explicitly state that the total area is represented by Ap+Ac+A+d, the Examiner is permitted to give a claim the broadest reasonable interpretation consistent with the specification. See MPEP § 2111. While it is true that Kim does not explicitly state the total area is represented by Ap+Ac+A+d, it is clear that Kim shows the following in the same manner as claimed: a) a dummy fine line pattern; b) main pad pattern; c) connection pad pattern; and d) main fine line pattern. It would have been obvious to one of ordinary skill in the art to allocate the claimed area to establish electrical communication between the chip and peripheral components since such technology was well known in the art at the time the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as obvious over Kim et al. (U.S. Patent No. 5,534,728) in view of Kamiyama et al. (U.S. Patent No. 5,322,764).

In regards to claim 2, Kim fails to disclose the following:

a) a width of the fine line pattern is below sub-micron.

However, Kamiyama et al. ("Kamiyama") discloses the width of the fine line pattern is below 1 *um* (For Example: See Column 10 Lines 18-30). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kim to include that the width of the fine line pattern is below 1 *um* as disclosed in Fontana because it aids in preventing side corrosion (For Example: See Column 8 Lines 48-55).

Additionally, since Kim and Kamiyama are both from the same field of endeavor, the purpose disclosed by Kamiyama would have been recognized in the pertinent art of Kim.

6. Claims 4, 7 and 11 are rejected under 35 U.S.C. 103(a) as obvious over Kim et al. (U.S. Patent No. 5,534,728) in view of Fontana et al. (*Corrosion Engineering*).

In regards to claim 4, Kim fails to disclose the following:

a) the plurality of metal wire patterns are made of aluminum or copper.

However, Fontana et al. ("Fontana") discloses the use of aluminum (For Example: See Section 5-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kim to include the use of aluminum as disclosed in Fontana because it aids in providing resistance to corrosion in many environments (For Example: See Section 5-9).

Additionally, since Kim and Fontana are both from the same field of endeavor, the purpose disclosed by Fontana would have been recognized in the pertinent art of Kim.

In regards to claims 7 and 11, Kim fails to disclose the following:

a) the plurality of metal wire patterns are made of aluminum or copper wire.

However, Fontana discloses the use of aluminum (For Example: See Section 5-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kim to include the use of aluminum as disclosed in Fontana because it aids in providing resistance to corrosion in many environments (For Example: See Section 5-9).

Additionally, since Kim and Fontana are both from the same field of endeavor, the purpose disclosed by Fontana would have been recognized in the pertinent art of Kim.

Conclusion

7. Applicant is advised that should claim 7 be found allowable, claim 11 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Crane et al. (U.S. Patent No. 3,838,984) discloses an interconnect for IC chips; b) Tashiro (U.S. Patent No. 5,042,147) discloses a surface mounted wiring board; c) Shiga (U.S. Patent No. 5,067,006) discloses a semiconductor device; d) Mizushima (U.S. Patent No. 5,404,045) discloses a semiconductor device; e) Lam (U.S. Patent No. 5,612,514) discloses a TAB test device; f) Kuwano (U.S. Patent No. discloses a single end out arrangement; g) Heo (U.S. Patent No. 5,926,733) discloses a metal layer pattern; h) Kang et al. (U.S. Patent No. 6,031,281) discloses a semiconductor device; i) Akram (U.S. Patent No. 6,064,116) discloses a device for electrically coupling; j) Drehobl et al. (U.S. Publication No. 2001/0002065) discloses an integrated circuit package; k) Umehara et al. (U.S. Patent No. 6,268,644) discloses a semiconductor device; l) Nakamura (U.S. Publication No. 2002/00241149) discloses a semiconductor device; m) Terauchi (U.S. Publication No. 2002/0079596) discloses a semiconductor device; n) Hara et al. (U.S. Patent No. 6,414,387) discloses a semiconductor device; o) Asada (U.S. Publication No. 2002/0163068) discloses a semiconductor device; p) *Investigation of Aluminum CMP to sub-quarter micron DRAM devices*;

q) *Pitting and Copper Accumulation Associated with Aluminum Cap*; and r) Murai et al. (Japanese Patent No. 411214522) discloses a wire layout.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

May 1, 2003

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